R E M A R K S

Reconsideration of this application, as amended, is respectfully requested.

The March 5, 2004 Office Action and the Examiner's comments have been carefully considered. In response, claims are cancelled and added, and remarks are set forth below in a sincere effort to place the present application in form for allowance. The amendments are supported by the application as originally filed. Therefore, no new matter is added.

SPECIFICATION

In the Office Action the Examiner indicates that the specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicants acknowledge the Examiner's request to correct any errors in the specification of which Applicants may become aware.

CLAIM OBJECTIONS

In the Office Action claims 16, 21 and 26 are objected to because of certain informalities. In response, claims 16, 21 and 26 are cancelled, thereby rendering the objection to these claims moot.

PRIOR ART REJECTIONS

In the Office Action claims 1-3 are rejected under 35 USC 102 as being anticipated by USP 4,348,762 (Shiun). Claims 7, 8 and 14 are rejected under 35 USC 103 as being unpatentable over Shiun. Claims 4-6 and 9-11 are rejected under 35 USC 103 as being unpatentable over Shiun in view of USP 6,215,513 (Ashikaga). Claim 12 is rejected under 35 USC 103 as being unpatentable over Ashikaga in view of USP 5,451,894 (Guo). Claim 13 is rejected under 35 USC 103 as being unpatentable over Ashikaga in view of the Guo. Claim 15 is rejected under 35 USC 103 as being unpatentable over Shiun in view of Ashikaga. Claims 16-31 are rejected under 35 USC 103 as being unpatentable over Ashikaga and Guo, and further in view of USP 6,127,858 (Stinson et al.).

In response, claims 1-31 are cancelled and new claims 32-46 are added.

New claims 32-46 correspond to the subject matter of the prior claims and are clearly supported by the written description and drawings as originally filed.

As recited in new claim 32, the clock generating device of the present claimed invention changes a clock frequency during a predetermined time. The clock generating device includes:

a reference clock generating section which generates a

reference clock having a fixed reference frequency;

a delay chain section which produces a plurality of delay clocks having different delayed phases respectively with the fixed reference frequency from the reference clock;

a switching control section to output a selection signal to indicate which is clock to be selected so as to change a clock frequency during a predetermined time; and

a selecting combining section to select and combine plural delay clocks so as to output composite pulses having a frequency different from the fixed reference frequency during the predetermined time in accordance with the selection signal.

As shown in Figs. 4(a) and 4(b), for example, when a character image and a photographic image are formed on the same sheet, imagewise exposure for a photoreceptor is conducted by scanning with a laser beam with different clock frequencies for two regions A and B. To accomplish this, it is necessary to change the clock frequency during a predetermined time on the region B in Fig. 4(a) (see the description at, for example, page 20, line 17 to page 21, line 18).

The present claimed invention enables the clock generating device to change a clock frequency during a predetermined time. The reference clock generating section generates a reference clock having a fixed reference frequency, as shown in Fig. 2(a).

The delay chain section produces a plurality of delay clocks having different delayed phases respectively with the fixed reference frequency from the reference clock, as shown in Figs. 2(b) to 2(n). The switching control section 440 in Fig. 1 outputs a selection signal to indicate which clock is to be selected so as to change a clock frequency during a predetermined time, as shown in Fig. 9(a) to 9(d). The selecting combining section selects and combines plural delay clocks so as to output composite pulses having a frequency different from the reference frequency during the predetermined time in accordance with the selection signal, as shown in Fig. 9(e).

Another embodiment is shown in Figs. 10(e) to 10(j) to make the frequency higher, lower or variable from the reference clock shown in Fig. 10(a).

As can be seen from Fig. 1 of Shiun, the reference merely teaches a switch control circuit 3 to select one of pulses differing in phase. Shiun does not, however, disclose, teach or suggest a structure to change the clock frequency. Accordingly, it is respectfully submitted that the present invention as recited in new claim 32 is not anticipated or rendered obvious by Shiun.

Ashikaga (see the abstract thereof) merely teaches a structure to control the width of a pulse. Ashikaga does not,

however, disclose, teach or suggest a structure to change the clock frequency as recited in new claim 32.

Guo (see the abstract thereof) merely teaches a structure to conduct a 360-degree phase shift. Guo does not, however, disclose, teach or suggest a structure to change the clock frequency as recited in new claim 32.

Accordingly, even if Ashikaga and Guo are taken in combination, the present claimed invention recited in new claim 32 is not anticipated or rendered obvious by the cited references.

Stinson et al. (see Fig. 5 thereof) merely teach a structure to generate a shrunk and/or stretched clock for a tester coupled to a microprocessor (see column 1, lines 41-57 thereof). Stinson et al. do not, however, disclose, teach or suggest a structure to change the clock frequency by using the delay chain section, the switching control section and the selecting combining section as recited in new claim 32. In fact, Stinson et al. employ PLL 202 shown in Fig. 2 thereof to change the clock frequency which was used in the prior art (see page 1, lines 14-17 of the present application).

In the present claimed invention, however, since the reference clock generating section generates a reference clock having a <u>fixed reference frequency,</u> the reference clock

generating section is quite different from a PLL circuit.

Accordingly, even if Ashikaga, Guo and Stinson were taken in combination, the present claimed invention as recited in new claim 32 would not have been obvious.

Claims 33-46 are either directly or indirectly dependent on claim 32 and are patentable over the cited references in view of their dependence on claim 32 and because the references do not disclose, teach or suggest each of the limitations set forth in claims 33-46.

In view of the foregoing, claims 32-46 are patentable over the cited references under 35 USC 102 as well as 35 USC 103.

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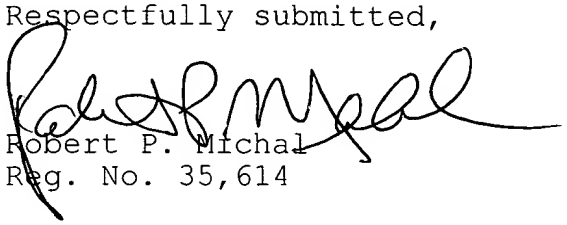
Entry of this Amendment, allowance of the claims and the passing of this application to issue are respectfully solicited.

If the Examiner disagrees with any of the foregoing, the Examiner is respectfully requested to point out where there is support for a contrary view.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned at the telephone number given below for prompt action.

Respectfully submitted,



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